REMARKS

Summary of Office Action

Claims 1-7, 11, and 12 stand rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Nishimura (US Pub. No. 2001/0002829) in view of Youn (US Pat. No. 5,856,816).

Claims 8 and 9 stand rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Nishimura, in view of Youn, and further in view of Applicant's alleged admittance of prior art.

Claims 14 and 15 stand rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Nishimura, in view of Youn, and further in view of Gooding et al. (US Pat. No. 4,580,265).

Summary of Amendment

Drawing Figure 12 and the Specification have been amended to correct inadvertent typographic errors. As no new matter or new issues have been introduced, entry of the amendments to the drawings and the specification is respectfully requested.

Claims 1-9 and 11-12 have been amended and new claims 16-20 have been added. No new matter has been entered.

Claims 1-9, 11-12, 14-20 are currently pending for consideration.

Information Disclosure Statement

An Information Disclosure Statement has been filed concurrently with the RCE for consideration.

All Claims Comply with §103

It is noted that the Office Action Summary form (Form PTOL-326) only lists claims 1-7, 11, and 12 as "pending" and "rejected." For the record, claims 1-9, 11, 12, 14, and 15 are actually pending and have been rejected in the final Office Action.

Claims 1-7, 11, and 12 stand rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Nishimura (US Pub. No. 2001/0002829) in view of Youn (US Pat. No. 5,856,816), claims 8 and 9 stand rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Nishimura, in view of Youn, and further in view of Applicant's alleged admittance of prior art, and claims 14 and 15 stand rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Nishimura, in view of Youn, and further in view of Gooding et al. (US Pat. No. 4,580,265). These rejections are respectfully traversed for the following reasons.

As amended, independent claim 1 recites, in part,

> a ***first*** data ***polarity*** inversion driver determining whether a first data transition has occurred in ***a first set*** of data, and inverting the polarity of the first set of data in accordance with the determined result; and
> a ***second*** data ***polarity*** inversion driver determining whether a second data transition has occurred in ***a second set*** of data and inverting the polarity of the second set of data in accordance with the determined result,
> wherein the ***first set*** of data is ***odd-numbered*** bits in the input data and the ***second set*** of data is ***even-numbered*** bits in the input data.

Similarly, amended independent claim 11 recites, in part,

> ***dividing input data*** into ***a first set*** of data and ***a second set*** of data;
> inputting the ***first and second sets*** of data to the ***first and second data polarity inversion drivers***, respectively...,
> wherein the ***first set*** of data is ***odd-numbered*** bits of the input data and the ***second set*** of data is ***even-numbered*** bits of the input data.

None of the art of record, whether taken individually or in combination, teaches at least these features.

Nishimura discloses a ***4-port*** polarity inverting circuit, i.e., PORT A-D (FIG.2; page 3, paragraph [0047], ln. 2). FIG. 2 shows data polarity inversion judgement/generation units 10-1 (PORT A) through 10-4 (PORT B), which means each unit 10-1 through 10-4 process ***one quarter (¼) of the data***. Nishimura, therefore, teaches that the ***first quarter*** of the data (i.e., BUS1-24) is input to PORT A (10-1), the ***second quarter*** of the data (i.e., BUS25-48) is input to PORT B (10-2), and so forth. Moreover, because each judgment/generation units 10-1 through 10-4 receives the input data in ***sequential order***, the each of the ports receives ***both even and odd*** numbered bits of input data. Therefore, Nishimura fails to teach or suggest first and second data polarity inversion drivers receiving first and second data, respectively, "wherein the ***first set*** of data is ***odd-numbered bits*** of the input data and the ***second set*** of data is ***even-numbered bits*** of the input data" as recited in independent claims 1 and 11.

Youn is not directed to a polarity inversion driver and is inapposite to the teachings in Nishimura. Youn is directed to an LCD driving circuit that divides the data signals to be applied to the ***pixels*** in half. Odd pixel data bits are latched into odd-latch 25 and even pixel data bits are latched into even-latch 26, the combination of which forms one horizontal pixel image, and the latched data are D/A converted before being applied to the ***pixels***. None of the odd/even data is input into "a first and second data ***polarity inversion drivers***" for "determining whether a first [and second] data transition has occurred" (claim 1) or "inputting the first and second sets of data to the first and second data ***polarity inversion drivers***, respectively" (claim 11) as recited in at

least independent claims 1 and 11. Thus, even if combined, Nishimura and Youn fail to disclose at least the above cited claim features.

Moreover, Applicant respectfully traverses the argument that "Youn teaches dividing the data into odd and even data portions, which remedies the deficiencies of Nishimura (FOA: page 7, paragraph 6)." As stated in MPEP §2143.01, "[t]he mere fact that reference can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination (citing to *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990))." In this case, there is no teaching or desirability to apply the ***odd/even*** divided data signals to ***be applied to the pixels*** as taught by Youn to the ***4-port polarity inversion circuit*** of Nishimura, especially given that Nishimura teaches inputting the data ***in sequential order*** into 4-ports. The Office Action fails to establish why or how one with ordinary skill in the art would apply odd/even divided driving data signals as taught in Youn into a 4-port polarity inversion circuit as taught in Nishimura. It is respectfully submitted that the mere fact Nishimura's teaching and Youn's teaching are generally related to driving LCD panels ***is not enough*** to motivate one with ordinary skill in the art to combine or modify Nishimura with Youn as asserted in the Office Action.

For at least these reasons, Nishimura and Youn, whether taken individually or in combination, fail to teach or suggest the features recited in independent claims 1 and 11, and accordingly, their dependent claims 2-9, 12, 14 and 15 as neither the Applicants' alleged admission of prior art nor Gooding et al. cures the indicated deficiencies above.

New Claims

New claims 16-20 recite the novel and non-obvious features discussed above. In particular, new independent claim 16 recites, in part, a "2-port data polarity inverter" that comprises "an odd data polarity inversion driver" and "an even data polarity inversion driver." As explained above, none of the prior art of record teach such features. New claims 17-20 are patterned after claims 2-9 and depend from new independent claim 16. Therefore, it is believed that no new matter has been added.

CONCLUSION

In view of the foregoing, reconsideration and timely allowance of the pending claims are respectfully requested. If there are any other fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-0310. If a fee is required for an extension of time under 37 C.F.R. 1.136 not accounted for above, such an extension is requested and the fee should also be charged to our Deposit Account.

Respectfully submitted,

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